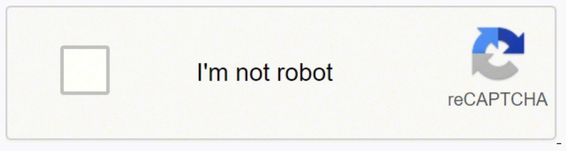

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Become a SystemVerilog Expert! You can verify complex designs thoroughly and quickly if you start with the right tools. This book teaches you the SystemVerilog constructs for verification with over 300 examples. Learn proven techniques so you can build testbenches that automatically generate stimulus to catch those bugs. The SystemVerilog language contains hundreds of new features. This book shows you how to use the important ones to get your job done. You will learn how to use techniques such as * Interfaces and clocking blocks * Object oriented programming * Constrained random stimulus * Functional coverage * Logical assertions "SystemVerilog for Verification is a MUST prerequisite book for anyone involved in the creation of SystemVerilog testbenches, as standalone or in a framework like Synopsys VMM. I consider this work as a golden reference as it gets into the inner use of the language and provides excellent insights into practical coding styles. This book fills a needed void in explaining, in a very readable manner and with lots of examples and visuals, the key elements and applications of thelanguage for a verification methodology that supports constrained-random testing in a transaction-based methodology." Ben Cohen, Author/Consultant/Trainer, abv-sva.org Chris Spear is a Verification Consultant for Synopsys, and has advised companies around the world on testbench methodology. He has trained hundreds of engineers on SystemVerilog's verification constructs. Chris is the author of the widely used File I/O PLI package for Verilog. Testbenches get more complex. You need this book to keep up! *** Includes over 300 examples *** Plus a foreword by Phil Moorby, creator of the Verilog language. SystemVerilog for Verification teaches the reader how to use the power of the new SystemVerilog testbench constructs plus methodology without requiring in-depth knowledge of Object Oriented Programming or Constrained Random Testing. The book covers the SystemVerilog verification constructs such as classes, program blocks, C interface, randomization, and functional coverage. SystemVerilog for Verification also reviews some design topics such as interfaces and array types. There are extensive code examples and detailed explanations. The book will be based on Synopsys courses, seminars, and tutorials that the author developed for SystemVerilog, Vera, RVM, and OOP. Concepts will be built up chapter-by-chapter, and detailed testbench using these topics will be presented in the final chapter. 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